Course Title: Computer organization and architecture **Credit: 3**
Course No: CSIT.211 **Number of period per week: 3+3**
Nature of the Course: Theory + Tutorial **Total hours: 45+45**
Year: Second, Semester: Third
Level: B. Sc. CSIT

1. Course Introduction

In this course the term architecture is taken to include instruction set architecture (the programmer's abstraction of a computer), organization or micro architecture (the internal implementation of a computer at the register and functional unit level), and system architecture (the organization of the computer at the cache, and bus level).

2. Objectives

At the end of this course the students should be able to:

- Understand computer representation of data
- Demonstrate algorithms used to perform different operations on the data
- Describe different operations in terms of Microoperations
- Describe architecture of basic computer
- Understand microprogrammed control unit
- Describe and memory and I/O organization of a typical computer system
- Understand benefits of pipelined and multiprocessor systems

3. Specific Objectives and Contents

Specific Objectives	**Contents**
• Understand how numbers and text can be represented in digital form and their limitations. • Understand concept of overflow and detection of overflow. • Appreciate how errors can be detected using parity bits.	**Unit I: Data Representation (4)** 1.1. Data Representation: Binary Representation, BCD, Alphanumeric Representation, Complements, Fixed Point representation, Representing Negative Numbers, Floating Point Representation, Arithmetic with Complements, Overflow, Detecting Overflow 1.2. Other Binary Codes: Gray Code, self Complementing Code, Weighted Code, Excess-3 Code, EBCDIC 1.3. Error Detection Codes: Parity Bit, Odd Parity, Even parity, Parity Generator & Checker
• Understand register transfer language • Describe arithmetic, logic and shift operations in terms of microperations.	**Unit II: Register Transfer and Microoperations (6)** 2.1. Overview: Microoperation, Register Transfer Language, Register, Register Transfer, Control Function 2.2. Arithmetic Microoperations: Binary Adder, Binary

• Build circuit diagrams of arithmetic, logic and shift operations.	Adder-Subtractor, Binary Incrementer, Arithmetic Circuit 2.3. Logic Microoperations, Hardware Implementation, Applications of Logic Microoperations. 2.4. Shift Microoperations: Logical Shift, Circular shift, Arithmetic Shift, Hardware Implementation of Shifter.
• Learn computer organization and architecture using hypothetical computer system. • Describe Common bus system of basic computer. • Interpret instruction set of basic computer • Describe interrupt cycle of basic computer • Understand overall execution cycle of basic computer	**Unit III: Basic Computer Organization and Design (7)** 3.1. Instruction Code, Operation Code, Stored Program Concept 3.2. Registers and memory of Basic Computer, Common Bus System for Basic Computer. 3.3. Instruction Format, Instruction Set Completeness, Control Unit of Basic Computer, Control Timing Signals 3.4. Instruction Cycle of Basic computer, Determining Type of Instruction, Memory Reference Instructions, Input-Output Instructions, Program Interrupt & Interrupt Cycle. 3.5. Description and Flowchart of Basic Computer
• Understand microprogram and microprogrammed control unit • Describe microprogram sequencer • Design microprogrammed control unit	**Unit IV:** Microprogrammed Control**(4)** 4.1. Control Word, Microprogram, Control Memory, Control Address Register,Sequencer 4.2. Address Sequencing, Conditional Branch, Mapping of Instructions, Subroutines, Microinstruction Format, Symbolic Microinstructions 4.3. Design of Control Unit
• Understand different CPU organizations • Describe types of instructions on the basic of number of operands • Interpret operand using addressing modes. • Compare and Contrast RISC and CISC computer architectures	**Unit V: Central Processing Unit (4)** 5.1. Major Components of CPU, CPU Organization (Single Accumulator Organization, General Register Organization, Stack Organization) 5.2. Instruction Formats, Addressing Modes, Data Transfer and manipulation, Program Control, Subroutine Call and Return, Types of Interrupt 5.3. RISC vs CISC, Pros and Cons of RISC and CISC Overlapped Register Windows
• Differentiate parallel processing from pipelining • Understand pipelining and speedup gain due to pipelining • Use pipelining with arithmetic operation • Describe problems in pipelining and list their possible solutions • Give basic idea behind vector processing	**Unit VI: Pipelining (5)** 6.1. Parallel Processing, Multiple Functional Units, Flynn's Classification 6.2. Pipelining: Concept and Demonstration with Example, Speedup Equation, Floating Point addition and Subtraction with Pipelining 6.3. Instruction Level Pipelining: Instruction Cycle, Three & Four-Segment Instruction Pipeline, Pipeline Conflicts and Solutions 6.4. Vector Processing, Applications, Vector Operations, Matrix Multiplication

• Describe addition, subtraction, multiplication and division algorithm for signed magnitude data • Demonstrate addition, subtraction and multiplication algorithm for signed 2's complement data • Understand hardware implementation of all described algorithms	**Unit VII: Computer Arithmetic (4)** 7.1. Addition and Subtraction with Signed Magnitude Data (Hardware Implementation and Algorithm), Addition and Subtraction with Signed 2's Complement Data 7.2. Multiplication of Signed Magnitude Data (Hardware Implementation and Algorithm), Booth Multiplication (Hardware Implementation and Algorithm) 7.3. Division of Signed magnitude Data (Hardware Implementation and Algorithm), Divide Overflow
• Understand interface between I/O devices and CPU. • Compare strobe and handshaking mechanism of data transfer • Describe modes of data transfer along with their pros and cons • Explain methods of handling prioritized interrupts • Differentiate DMA from input-output processors	**Unit VIII: Input Output Organization (4)** 8.1. Input-Output Interface: I/O Bus and Interface Modules, I/O vs Memory Bus, Isolated vs Memory-Mapped I/O 8.2. Asynchronous Data Transfer: Strobe, Handshaking (Source and Destination Initiated) 8.3. Modes Of Transfer: Programmed I/O, Interrupt-Initiated I/O, Direct memory Access 8.4. Priority Interrupt: Polling, Daisy-Chaining, Parallel Priority Interrupt 8.5. Direct Memory Access, Input-Output Processor, DMA vs IOP
• Understand why a memory hierarchy is necessary to reduce the effective memory latency. • Appreciate that most data on the memory bus is cache refill traffic • Describe techniques of mapping data stored in RAM to the data in cache memory	**Unit IX: Memory Organization (4)** 9.1 Memory Hierarchy, Main Memory, RAM and ROM Chips, Memory address Map, Memory Connection to CPU, Auxiliary Memory (magnetic Disk, Magnetic Tape) 9.1 Associative Memory: Hardware Organization, Match Logic, Read Operation, Write Operation 9.1 Cache Memory: Locality of Reference, Hit & Miss Ratio, Mapping (Direct, Associative, Set Associative), Write Policies(Write-Back, Write-Through)
• Understand how performance can be increased by incorporating multiple processors on a single chip. • Appreciate the need for cache coherency in multiprocessor systems	**Unit X: Multiprocessors (3)** 10.1 Overview, Loosely Coupled & Tightly Coupled multiprocessors, Interconnection Structures 10.1 Interprocessor Arbitration (Serial , Parallel and Dynamic), Interprocessor Communications and Synchronization **10.1** Cache Coherence, Solution to cache Coherence Problem

Evaluation System

<table>
<tr><th colspan="8">Undergraduate Programs</th></tr>
<tr><th>External Evaluation</th><th>Marks</th><th>Internal Evaluation</th><th>Weight age</th><th>Marks</th><th>Viva-voce</th><th>Weight age</th><th>Mark</th></tr>
<tr><td>End semester examination</td><td rowspan="4">60</td><td>Assignments</td><td>20%</td><td rowspan="4">20</td><td>Report and Presentation on any topic</td><td>50%</td><td rowspan="4">20</td></tr>
<tr><td>(Details are given in the separate table at the end)</td><td>Quizzes</td><td>10%</td><td>Presentation</td><td>25%</td></tr>
<tr><td></td><td>Attendance</td><td>20%</td><td>Viva</td><td>25%</td></tr>
<tr><td></td><td>Internal Exams</td><td>50%</td><td></td><td></td></tr>
<tr><td>Total External</td><td>60</td><td>Total Internal</td><td>100%</td><td>20</td><td></td><td>100%</td><td>20</td></tr>
<tr><td colspan="8">Full Marks 60+20+20 = 100</td></tr>
</table>

External evaluation:

1. **End semester examination:**
   It is a written examination at the end of the semester. The questions will be asked covering all the units of the course. The question model, full marks, time and others will be as per the following grid.

2. **External Evaluation (Viva):**
   After completing the end semester theoretical examination, viva examination will be held. External examiner will evaluate report/presentation & take viva exam and will do above mentioned evaluation. Students should make a small report by relating any of the studied topics in the subject to some application areas/examples. Reports can be made in groups. There will be an internal examiner to assist the external examiner. In this examination Students must demonstrate the knowledge of the subject matter.

Full Marks: 100, Pass Marks: 45, Time: 3 Hrs

Nature of question	Total questions to be asked	Total questions to be answered	Total marks	Weightage
Group A: multiple choice*	20	20	20×1 = 20	60%
Group B: Short answer type questions	8	6	6×8 = 48	60%
Group C: Long answer type question/long menu driven programs	3	2	2×16 =32	60%
			100	100%

Each student must secure at least 50% marks in internal evaluation in order to appear in the end semester examination. Failed student will not be eligible to appear in the end semester examinations.

Internal evaluation

Assignment: Each student must submit the assignment individually. The stipulated time for submission of the assignment will be seriously taken.

Quizzes: Unannounced and announced quizzes/tests will be taken by the respective subject teachers. Such quizzes/tests will be conducted twice per semester. The students will be evaluated accordingly.

Attendance in class: Students should regularly attend and participate in class discussion. Eighty percent class attendance is mandatory for the students to enable them to appear in the end semester examination. Below 80% attendance in the class will signify NOT QUALIFIED (NQ) to attend the end semester examination.

Presentation: Students will be divided into groups and each group will be provided with a topic for presentation. It will be evaluated individually as well as group-wise. Individual students have to make presentations on the given topics.

Mid-term examination: It is a written examination and the questions will be asked covering all the topics in the session of the course.

Discussion and participation: Students will be evaluated on the basis of their active participation in the classroom discussions.

Instructional Techniques: All topics are discussed with emphasis on real-world application. List of instructional techniques is as follows:

- Lecture and Discussion
- Group work and Individual work
- Assignments
- Presentation by Students
- Quizzes
- Guest Lecture

Students are advised to attend all the classes and complete all the assignments within the specified time period. If a student does not attend the class(es), it is his/her sole responsibility to cover the topic(s) taught during that period. If a student fails to attend a formal exam/quiz/test, there won’t be any provision for re-exam.

Prescribed Text

- *M. Morris Mano*, “Computer System Architecture”, Prentice-Hall of India, Pvt. Ltd., Third edition, 2007

References

- *William Stallings*, “Computer Organization and Architecture”, Prentice-Hall of India, Pvt. Ltd., Seventh edition, 2005.
- *Vincent P. Heuring and Harry F. Jordan*, “Computer System Design and Architecture”, Prentice-Hall of India, Pvt. Ltd., Second edition, 2003.